Chapter I
INTRODUCTION

Novel electronic applications often require high quality single crystalline layers on appropriate substrates. Various methods such as heteroepitaxial growth by molecular beam epitaxy or metalorganic chemical vapour deposition yield devices with a high concentration of threading dislocations when involving materials with different lattice constants such as silicon and gallium arsenide.

Wafer bonding is an attractive, flexible choice for the fabrication of such single crystalline layers on top of substrates in terms of doping profiles, surface orientation, crystallographic alignment and lattice mismatch [1]. The phenomenon of adhesion between two smooth and clean surfaces by means of van der Waals forces was observed and investigated more than one century ago. However, it was not until the mid eighties of the last century that researches from IBM and Toshiba introduced the hydrophilic and hydrophobic bonding between silicon wafers for electronic applications [2], [3]. In their approach the initial low bonding strength had to be increased to the fracture energy of the bulk material by high temperature annealing steps. In many situations a high bonding energy is desired directly after room temperature bonding, and this could be achieved after appropriate surface activation and bonding in an ultra-high vacuum (UHV) environment. Using this approach which was termed ultra-high vacuum bonding, high fracture energies could be achieved upon joining at room temperature by covalent bonding [4]. However, except for a few material combinations that have been shown to work very well, the aforementioned technique remains a challenge due to different surface chemistries specific to each material. Particularly, when bonding silicon to gallium arsenide at room temperature, low fracture energies were reported necessitating high temperature annealing before further processing could be carried out. In order to overcome the problem of different thermal expansion coefficients, heteroepitaxial growth of silicon and gallium arsenide on different substrates in combination with wafer bonding were used, as in the case of silicon-on-sapphire bonded to gallium arsenide [5] and gallium arsenide-on-germanium bonded to silicon [6]. Nevertheless, such approaches tend to be tedious and expensive. To our knowledge, no direct bonding of silicon to gallium arsenide without intermediate layers on a large scale was reported up to date.

It is within the scope of the present work to demonstrate that smooth, oxide-free interfaces can be obtained by UHV bonding of silicon to gallium arsenide at room temperature. Electrical and structural investigations were carried out in order to demonstrate the suitability of such interfaces for device fabrication.

Since most applications require uniform layers in the micron and sub-micron thickness range on appropriate substrates, it is necessary to develop a method that would allow reducing the device thickness effectively, without sacrificing the whole wafer. Chemo-mechanical polishing and selective etching techniques are

obviously not the best choice in this respect, both being time consuming, expensive and cumbersome. Layer transfer by means of implantation induced splitting combined with wafer bonding is already a well-established procedure for producing silicon-on-insulator wafers [7]. Nevertheless, it always involves an intermediate oxide layer which makes this approach unsuitable for applications requiring electrically conductive interfaces.

In the present work a novel layer transfer approach based on ion implantation, surface activation by photons in the ultra-violet range and UHV bonding is proposed and implemented for the transfer of ultra-thin single crystalline silicon and GaAs layers onto silicon substrates.

Although UHV bonded interfaces are oxide-free, the current flow across the interfaces can still be hindered to some degree by the presence of a grain boundary formed during bonding. Previous investigations have shown that the Si-Si bonding process causes a potential barrier at the fused interface, particularly important in lowly doped substrates [8]. However, up to now little attention has been paid to the electrical properties of bipolar interfaces produced by UHV bonding, especially those involving dissimilar materials.

The dissertation consists of five chapters. Following the introduction, Chapter II deals with the basic concepts of wafer bonding, ion implantation and layer splitting. An overview of the defects present in crystalline semiconductors is presented, with emphasis on grain boundaries. The anti-serial Schottky barrier model used to describe the thermionic emission over the unipolar grain boundary barrier [9] is briefly discussed, followed by a description of the drift-diffusion model augmented to include interface traps, which was used to model bipolar interfaces.

Chapter III is dedicated to the experimental work performed in this dissertation. The complete process flow including ion implantation, cleaning, surface activation, UHV bonding and sample preparation is described. An overview of investigation techniques is also given.

Chapter IV focuses on results and discussions. The electrical properties are investigated by means of temperature-dependent current-voltage measurements and deep-level transient spectroscopy. The results are correlated with numerical simulations of the fabricated devices in order to understand the physical processes governing the electrical transport across bonded interfaces between identical and dissimilar materials. The layer transfer of Si and GaAs layers onto silicon substrates using the proposed approach is shown to work very well, yielding devices with good structural and electrical properties.

Finally, a summary of the work is given in Chapter V.