Chapter III
EXPERIMENTS

3.1. Materials used in the experimental study

According to the theoretical investigations presented in the previous chapter, the bonding process causes both a potential barrier and G-R centers at the interface with important consequences for the electrical properties of the fabricated devices. The impact of the interface on the current-voltage characteristics should be more pronounced in unipolar devices since in that case the occupation of interface states increases when the device is biased, opposite to the bipolar case. Impurities and material imperfections can further influence the properties of the devices.

The objective of this work is the investigation of the steady-state and transient electrical behaviour of unipolar and bipolar devices fabricated by UHV bonding. Special attention has been given to the possibility of combining ion implantation with UHV bonding in order to induce transfer of ultra-thin layers onto silicon substrates. High quality single-crystalline Si and GaAs wafers mainly (100) oriented were used to fabricate homo- and heterojunctions. The wafer diameter was 100 mm in all cases and the thickness was 525 μm ± 25 μm and 625 μm ± 25 μm for Si and GaAs wafers, respectively. The doping of the Si wafers was in the range 10^{14}-10^{18} cm^{-3} for both n and p-type wafers. The GaAs wafers were n-type doped, in the range 10^{17}-10^{18} cm^{-3}.

The implantations were performed by the company Implant Sciences located in USA. In all cases, the implantation was performed at RT using a 7° tilt of the beam with respect to a direction perpendicular to the wafer surface (see Section 2.2.1, Chapter II). Different energies and doses listed in Table 3.1 were used in order to determine the optimal conditions for achieving large-scale transfer.

Implanted species	Energy (keV)	Dose (x10^{16} ions/cm^2)	Target	
			Material	Doping (cm^{-3})
H_2^+	30	1.5	(111)Si	$3x10^{14}$ (n)
H_2^+	30	1.5	(100)Si	$1x10^{15}$ (p)
H_2^+	30	1.8	(100)Si	$1x10^{15}$ (p)
H_2^+	130	5	(100)Si	$4x10^{17}$ (p)
H_2^+	130	5	(111)Si	$6x10^{14}$ (n)
He^+	60	3	(100)GaAs	$5x10^{17}$ (n)
He^+	60	5	(100)GaAs	$5x10^{17}$ (n)

Table 3.1: Implantation conditions for layer transfer experiments.

The Si wafers were capped before implantation with a thermally grown SiO_2 layer (thickness around 50 nm) for protection. The GaAs wafers had no protection except for their native oxides.

3.2. Wafer cleaning

3.2.1. Cleaning of silicon surfaces

In the case of silicon, the cleaning sequence follows the steps described in Section 2.1.2, Chapter II. The procedure was carried out in a conventional chemical lab (in a fume hood) using high purity quartz jars (for RCA1 and RCA2) and Teflon vessels (for HF dipping). The wafers were handled using Teflon tweezers and holders. VLSI (very large scale integration) grade chemicals were used together with ultrapure DI-water (resistivity 18 MΩcm) with TOC content (total organic contaminants) of 5-10 ppb. A particle filter at the nozzle of the purifying system ensures that the DI-water is free of particles larger than 0.22 μm.

The whole handling equipment was cleaned with RCA1 before coming in contact with the wafers, in order to remove dust particles and organic contamination. After thorough water rinse, the wafers undergo RCA1 and RCA2 cleaning for 10-15 min at 75-80°C. Since implanted wafers frequently exhibit a layer with dark-brown colour (probably due to implantation induced polymerisation of the contaminants present in the implanter chamber), additional H_2SO_4:H_2O_2 cleaning in an ultrasonic bath is performed before RCA1.

Hydrophilic bonding was performed only for training purposes and it is not within the scope of this work. Therefore, RCA cleaning was followed by HF dipping in order to remove the native (or thermally grown) oxide. Typical HF concentrations in H_2O of 2-5% and dipping times of 0.5-2 min were sufficient to completely remove the oxide without Si etching. Since the cleaning/handling was not performed in a cleanroom, it was essential to minimize as much as possible the exposure time of the hydrophobic surfaces before pre-bonding. The microcleanroom setup used for hydrophilic bonding [12] required the wafers to be dipped in succession (one after another) and introduced relatively long delays during which surfaces got contaminated. Therefore, another approach was used in order to decrease the delay to 5-10 sec. A T-shaped Teflon holder was designed in such a way to keep two wafers face to face during dipping using a pair of spacers. As soon as the wafers were taken off the solution, the spacers were removed and the wafers were pressed against each other in order to initiate the bonding. The bonding quality still showed some unavoidable scattering; sometimes the pre-bonding could not be achieved at all. Nevertheless, in this way the hydrophobic surfaces could be quickly protected before being transferred to the UHV assembly.

3.2.2. Cleaning of gallium arsenide surfaces

When cleaning GaAs surfaces, difficulties arise due to the partially ionic character of the Ga-As bonding which reflects in a lower stability of GaAs compared to Si. Because of this, GaAs surfaces are prone to decomposition

upon wet chemical cleaning. Trials to remove native oxides and contamination using standard RCA cleaning result in roughness that renders the wafer inappropriate for bonding. Moreover, GaAs does not have a well defined native oxide, the composition and thickness varying as a function of storage conditions and initial surface treatment. It is generally accepted that As_2O_x (with x=1, 3 and 5), Ga_2O_3 and $GaAsO_4$ can be found in different proportions on GaAs surfaces [1], [80], [81].

The standard method used to remove organics [82] relies on the ability of organic solvents such as trichloroethylene, acetone and ethanol to dissolve hydrocarbons. However, water rinse with ultrasonic waves, needed as a final step, can roughen the surface to some degree. For this reason, an approach based on ozone cleaning was used instead [83]. The wafers were exposed to ultra-violet radiation generated by a 172 nm Xe_2 lamp in low oxygen pressure. Contamination removal is accompanied by an increase of the oxide thickness with exposure time: As_2O_5 and Ga_2O_3 grow linearly as a function of time, while As_2O_3 grows logarithmically [84].

A decrease of the treatment time from 60 minutes to 1-2 minutes could be achieved using only O_2 gas; thus O^- radicals were involved in the cleaning process along with O_3, since they appear to be more reactive to organic contaminants than ozone itself. On the other hand, it is well known that O_2 molecules absorb strongly electromagnetic radiation with wavelengths between 130 and 175 nm [85]. By letting the absorption length be of the same order of magnitude as the distance of the UV lamp to the wafer, the O^- radicals near the wafer surface had a chance to react with adsorbed organic molecules. This was achieved by adjusting the O_2 pressure to 20 mbar, adding N_2 up to atmospheric pressure since the UV lamp did not work at very low pressures. These settings ensure an absorption length of ca. 10 cm, equal to the distance of the lamp to the wafer.

After UV/O_3 degreasing, the wafers were transferred to the UHV assembly.

3.3. Bonding procedure

3.3.1. The UHV system

All bonding experiments were performed using the UHV assembly developed by A. Plössl and H. Stenzel. The system is designed for 100 mm wafers. It consists of several vacuum chambers with various functionalities connected to a main transfer chamber, which contains a mechanism used to move the wafers from one chamber to another.

Once the wafers were cleaned and pre-bonded, they were transferred to the UHV assembly and processed in a few steps. First, the wafer pairs were inserted in a so-called load-lock chamber which was used as a buffer between ambient atmosphere and UHV. After the pressure reached a sufficiently low value ($<10^{-8}$ mbar) the flange interconnecting the load-lock and the next chamber was opened. The wafer pairs were transferred into the splitting chamber where they were separated using four disk-shaped knives. Afterwards, the wafers could be transferred to any of the chambers via the main transfer. A small turning chamber allows 180° rotation of the wafers (from ‘face up’ to ‘face

down' and vice-versa) followed usually by hydrogen desorption inside the heating chamber which could withstand temperatures up to 750°C. The wafers were maintained in a storage chamber which is endowed with a low-energy electron diffraction (LEED) system. Different layers (Au, Pt, Dy, Fe, Co) could be deposited onto wafer surfaces with the help of four small e^--beam sources and one large e^--beam unit. The processing of GaAs wafers (heating, atomic H bombardment) was performed in a separate chamber where also UV laser photodesorption experiments were done. Finally, a bonding chamber encloses a special mechanism which allowed bonding with a twist accuracy of ±1°. The bonding chamber is also endowed with a small heater for intermediate temperatures (as high as 400°C).

The pressure in all chambers is maintained below $1x10^{-10}$ mbar using a combination of turbo-molecular and ion-getter pumps. The partial pressure during experiments inside the GaAs chamber and the heating chamber is monitored by two quadrupole mass spectrometers (QMS) connected to a PC.

3.3.2. Silicon-silicon bonding

As discussed in Section 2.1.5 Chapter II, the RT covalent bonding requires activation of the surfaces by hydrogen desorption. This was done inside the heating chamber by heating to about 500°C at a rate of 5K/min followed by natural cooling to RT. Afterwards the wafers were transferred to the bonding chamber, where they were placed horizontally on top of each other, face to face, at a distance of about 5 mm. A mechanism operated by a lever releases the upper wafer causing it to fall on the lower one. The RT bonding occurred instantaneously as the wafers join together.

In order to study the influence of the bonding temperature on the electrical properties of the interfaces, the wafers were heated to about 200-250°C before bonding, using high power lamps placed outside the bonding chamber, the heat propagating inside through a 100 mm viewport.

The standard thermal desorption procedure could not be applied to implanted wafers, since the implantation induced splitting/blistering is a thermally activated process (Section 2.2.4, Chapter II). The conditions used for standard thermal desorption would destroy the surface quality due to onset of blistering, rendering it unbondable. Instead, a photothermal desorption approach was used by means of short laser pulses [86]. A KrF excimer laser having a wavelength of 248 nm and pulse width of 20 ns yielded energy densities between 60 and 1500 mJ/cm^2, corresponding to focused and unfocused conditions, respectively. The beam was supplied to the vacuum chamber via a quartz viewport under 45° incidence. Both single-shot and multi-pulse regimes were used (pulse frequency 1-10 Hz). After photothermal desorption, the implanted wafer was bonded to a handle wafer whose surface was activated as described in Section 2.1.5, Chapter II. After bonding, annealing experiments were performed in order to induce splitting following the process flow described in Fig. 2.5, Chapter II.

3.3.3. Silicon-gallium arsenide bonding

Due to reasons already outlined, GaAs surfaces were still covered with a thin oxide layer upon entering the UHV assembly.
Therefore, in order to achieve direct covalent boding of Si to GaAs the oxide has to be removed first.

The possibility of oxide removal by pure thermal means was initially studied since it was known that most of the oxide species present on the surface are quite volatile, leaving the surface at temperatures lower than 400°C, except for Ga_2O_3 which requires about 570°C to evaporate [81], [87]. Since this temperature is close to the range where GaAs undergoes decomposition due to massive arsenic evaporation, an alternative approach based on low energy atomic H bombardment was investigated [88], [89]. The atomic hydrogen beam was produced by feeding molecular hydrogen through a tantalum capillary heated by electron bombardment to 1800 - 2100 K. According to [90], this temperature is sufficient to achieve nearly total H_2 dissociation under relevant working pressures ($1x10^{-6}$ mbar inside the chamber and higher in the capillary). The wafers were heated during bombardment to temperatures of 300-600°C using exposure times between five minutes and one hour.

After oxide removal, the GaAs wafers were transferred into the bonding chamber and bonded at RT to silicon wafers whose surfaces were activated according to the procedure described in Section 2.1.5, Chapter II. The bonding procedure follows the process flow described in Fig. 3.1.

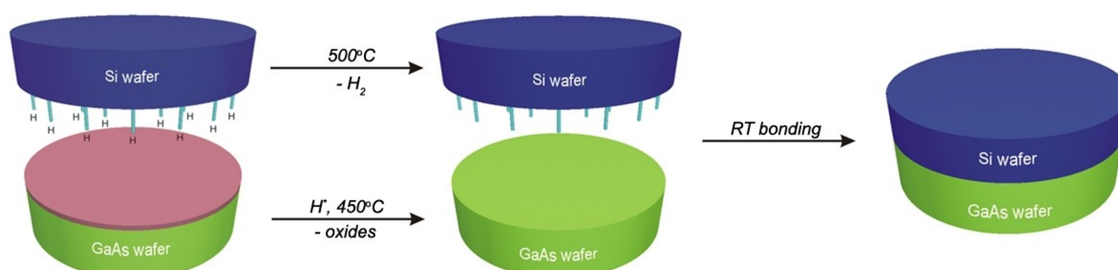

Figure 3.1: Schematic representation of the Si-GaAs RT bonding

For implanted GaAs wafers the oxide removal was attempted using the same photothermal desorption approach by means of excimer laser pulses. In order to avoid blistering and/or material ablation during laser irradiation, the energy density was kept to lower values compared to the case of silicon, i. e. 60-120 mJ/cm^2. Both single-shot and multi-pulse regimes were used.

3.4. Annealing experiments

When the temperature of a semiconductor material is increased sufficiently, it is expected that atoms start to move in the crystal lattice. This is particularly important at grain boundaries, where migration and interdiffusion could lead to a more relaxed interface. In implanted specimens, annealing can partially heal the implantation damage.

Si-Si interfaces were annealed at 1000°C in H_2 atmosphere (pressure 1 bar). The annealing was done in a quartz furnace for 5 hours. A temperature ramp of 30 K/min was used during heating and cooling.

For Si-GaAs interfaces, two kinds of annealing experiments were performed. In the case of Si-GaAs samples prepared by bonding, the GaAs layer had to be partially etched from 600 μm to about 20 μm using a H_2SO_4:H_2O_2:H_2O=8:1:1 mixture. The layer thickness was further reduced from 20 to 5 μm using chemo-mechanical polishing (CMP) with Syton. This was done in order to allow the samples to withstand the stress related to the difference in thermal expansion coefficients of the two materials. The samples were enclosed in a quartz ampoule after the air was evacuated to a pressure of $1x10^{-5}$ mbar. To ensure an arsenic overpressure during annealing, a large piece of GaAs was placed on top of the Si-GaAs sample before sealing the ampoule. The samples were heated to 850°C for 30 min using a temperature ramp of 10K/min.

In the case of Si-GaAs samples prepared by layer splitting, the thinning down step was not necessary, since the thickness of the transferred GaAs layer was in the range 0.4-0.6 μm. The annealing was performed in a quartz furnace at 850°C for 30 min in H_2 atmosphere (pressure 1 bar) using a temperature ramp of 10 K/min.

3.5. Investigation of the bonding quality

The first and most used investigation tool for analysis of bonding interfaces is the transmission infrared imaging. Apart of being straightforward and quick, it allows the inspection of a whole wafer pair in one step. It can be applied to both pre-bonded and UHV bonded pairs and relies on the property of silicon (and other semiconductors) of being transparent to infrared light. As a consequence, a first limiting factor is given by the fact that the band gap of the investigated semiconductor must be higher than the photon energy of the incident light. Silicon is transparent to wavelengths between 1200 and 1800 nm [91], provided that the doping level doesn't exceed 10^{19} cm^{-3}.

The system consists of an infrared light source and a CCD camera. The pair to be investigated is introduced between the source and the camera allowing the detection of the transmitted light and the storage of the resulting image.

The method is attractive especially for pre-bonded wafers in order to estimate the amount of macroscopic particles trapped at the interface, since they will clearly appear surrounded by dark areas as depicted in Fig. 3.2 (left). Light interference at unbonded areas produces fringes which appear as dark rings in the transmitted beam (Fig. 3.2, right). The features of these interference fringes allow the determination of the local separation between the wafers [92]. It is possible to combine the infrared imaging method with the double cantilever beam test [93], in order to estimate the bonding energy between the wafers. In this method, a blade of thickness *2h* is inserted at the bonded interface so as to debond an area of crack length *c*. At equilibrium, the elastic strain energy in the bended wafers equals the work of adhesion *W* required to form two new surfaces through the extension of the crack:

$$W = \frac{3Eh^2d^3}{4c^4} \tag{3.1}$$

with d being the wafer thickness and E denoting Young's modulus in the direction of the crack propagation.

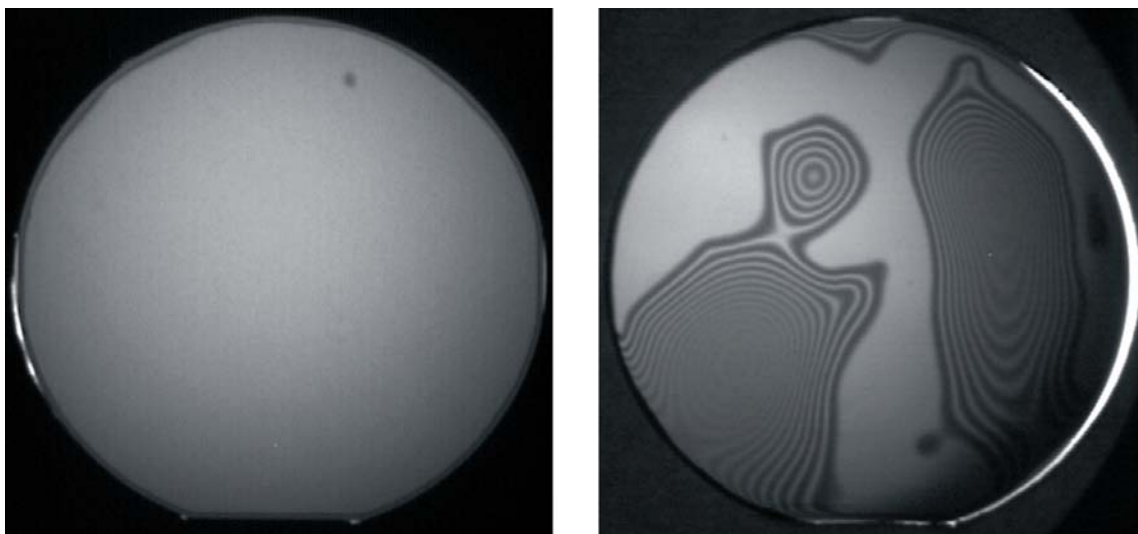

Figure 3.2: Infrared transmission image of a nearly-perfect bonded interface (left) and an interface featuring large unbonded areas (right).

Due to its simplicity and low demands, the infrared imaging is still very popular and was also used in this study to investigate bonded pairs at different processing stages. However, details smaller than 1 mm cannot be properly visualised with this method. An improved lateral resolution can be achieved using scanning acoustic microscopy [94], which in turn requires higher bonding energies to ensure stability of the wafer pair when immersed in the liquid required for transmitting the ultrasounds to the bonded wafer pair.

3.6. Electrical characterization

3.6.1. Sample contacting

After bonding the wafer pairs were transferred to the platinum chamber and/or to the e^--beam chamber for contacting. Ohmic contacts were prepared by e^--beam evaporation of Pt (on p-type substrates) and Sb (on n-type substrates) followed by Al deposition done in an external unit. Pt reacts with Si forming Pt_2Si which exhibits a low Schottky barrier height on p-type Si [95]. Sb is a doping element for Si and increases locally the substrate doping, creating an Al-Si tunnelling contact. Unfortunately Sb is quite volatile, developing a vapour pressure of 10^{-8} mbar at 280°C and can contaminate the e^--beam chamber. For this reason it was subsequently replaced with Dy which develops the same vapour pressure at 625°C and forms a silicide with low barrier on n-type silicon [96].

For GaAs substrates, Sn/Al and Ge/Au/Al tunnelling and alloyed contacts were prepared.

In some cases the ohmic contacts could not be prepared directly after bonding because the wafer pairs needed to be removed from the UHV assembly and undergo different processing steps (e. g. splitting experiments). After a quick cleaning step meant to remove particles and contaminants (a H_2SO_4:H_2O_2=3:1 mixture for Si-Si samples and acetone/ethanol/DI-water for Si-GaAs samples) the native oxides were removed by HF and HCl dip for Si and GaAs substrates, respectively. The samples were mounted on a disk shaped holder and were transferred to UHV where the metallization was done as described in the previous paragraph.

The quality of the contacts was influenced to a high degree by the surface cleanliness right before metallization and by the substrate doping.

3.6.2. Lock-in Thermography

Lock-in Thermography is a technique which allows a fast mapping of the current crossing the interface in terms of thermoelectric responses coming from different regions of the interface when a periodic current is applied to the bonded wafer pair. This type of excitation generates a broad spectrum of thermal wave frequencies having different penetration depth (proportional to the wavelength) and phase angle. Higher Fourier components are damped away, only the fundamental frequency being dominant and giving a thermoelectric signal.

The heat radiated by the wafer pair was detected at each 5 ms by a highly sensitive infrared camera endowed with an InSb sensor, being correlated with a sine and cosine wave synchronised to the exciting voltage signal. Thus it was possible to determine the amplitude and phase image of the heat distribution across the bonding interface [97]. The depth of the detected heat signal can be determined using the phase image. The frequency of the applied voltage must be tuned to make sure that the signal comes from the bonded interface and not from the ohmic contacts.

Typical DC voltages up to 1 V were applied to the samples (both forward and reverse in case of diodes). The current source was switched on and off by the lock-in electronics with frequencies of 3-30 Hz. In order to ensure the uniformity of the electrical contact, the metalized wafer surfaces were covered with a thin nickel foil and were enclosed into a black cover which was evacuated using a vacuum pump. Thus, contact discontinuities due to air bubbles were avoided. Typical heat amplitudes up to 5 mK were generated at the bonded interfaces. The brighter the amplitude image, the higher the current densities flowing across the interfaces.

3.6.3. Current-Voltage measurements

Current-voltage (I-V) measurements were performed using the four-point probe technique [78]. For this purpose, 3x1 mm^2 rectangular shaped samples were cut after metallization according to Fig. 3.3.

In order to arrange the four contacts, two channels 200 μm deep were cut on both sides of the bonded interface using a diamond wire saw. The samples were mounted on a transistor holder so as to have the four contacts pointing sideways. A thin dielectric plate was glued on top of the transistor holder before mounting the sample in order to avoid a short-circuit between the contacts. The connection between the holder pins and the sample has been done using silver paste and thin copper wires.

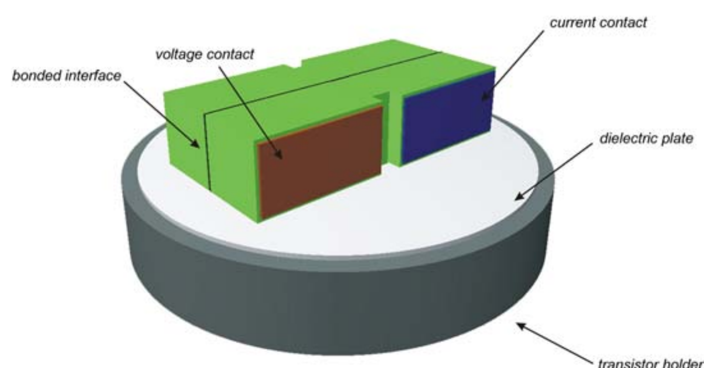

Figure 3.3: Sample configuration for four-point measurements.

Two contacts on each side of the interface were used to carry the current provided by a HP modular DC source. The voltage drop was measured at the other two contacts using a Keithley 2000 multimeter. In this way the effect of the contact resistance was minimized, only the interface being measured.

The transistor holder was mounted inside a copper block belonging to a nitrogen cooled cryostat. Using a computer controlled heating unit, measurements between 77 K and 370 K were possible. Typical voltages ranging from -0.5V to 0.5V were applied during measurements, but higher values were also possible.

In the case of samples prepared by layer transfer, only a two-point probe setup was used for simplicity. The contacting was done using a mask where 0.1 mm diameter holes were cut using a CO_2 laser. The metallization was done according to the method described in Section 3.6.1. The sample mounting was similar to the four-point setup, each contact being used both as a current and voltage probe.

3.6.4. DLTS

Deep level transient spectroscopy (DLTS) was introduced by Lang in 1974 [98] as a novel, highly sensitive method for the study of deep levels in semiconductors. Since then many extensions such as Double-Correlation DLTS (D-DLTS) [99], Constant-Capacitance DLTS (CC-DLTS) [100], Lock-in DLTS [101], Optical DLTS [102] and Laplace DLTS [103] have been introduced. The conventional DLTS technique and the experimental procedure will be discussed here. For an extensive study, the reader should refer to [78], [104] instead.

The principle of DLTS is to perturb the trap occupancy by changing the value of the reverse bias applied to a Schottky diode or p-n junction. The trap

concentration N_T and the activation energy of the defect E_A are related to the capacitance variation with time. By varying the filling pulse width, one can also study the capture process.

In order to point out the correspondence between the capacitance transient and the properties of the trap, we recall the equation describing the trap occupancy n_T as a function of time (2.33) as:

$$\frac{\partial n_T}{\partial t} = (c_n n + e_p)(N_T - n_T) - n_T(e_n + c_p p) \tag{3.2}$$

Consider a Schottky diode on an n-type substrate in thermal equilibrium. Assuming an acceptor-like level of density N_T positioned at E_T in the band gap, the dominant process will be the capture of electrons from the conduction band and $n_T \approx N_T$, provided that $n>>p$, $c_n>>c_p$ and $E_T < E_F$.

As soon as the device is biased to a value $-V_R$ electrons will be emitted from traps situated above the Fermi level. Equation (3.2) can be simplified leading to the following solution for n_T:

$$n_T(t) = n_T(0)e^{-e_n t} \approx N_T e^{-e_n t} \tag{3.3}$$

which states that all the trap occupancy follows an exponential decay, going to zero after sufficiently long time. If the device is pulsed between $-V_R$ and a value $-V_P$ ($-V_R < -V_P$), the traps will be filled again with electrons according to:

$$n_T(t) = N_T - [N_T - n_T(0)]e^{-c_n n t_f} \tag{3.4}$$

with t_f being the capture or filling time. For long times, all traps will be filled again with majority carriers as in the initial state. Therefore, by pulsing the device repetitively between $-V_R$ and $-V_P$ one can successively charge/discharge the traps, the magnitude of the charge depending on the total available traps N_T, on their emission/capture probabilities e_n, c_n and on the filling time t_f.

The charge variation associated with the change of the trap occupancy leads to a variation of the device capacitance defined as:

$$C = \frac{dQ}{dV} = \frac{\varepsilon A}{W} \tag{3.5}$$

Q being the fixed charge in the depletion region and W the width of the depletion region. The time-dependent junction capacitance is:

$$C(t) = \sqrt{\frac{\varepsilon A \rho(t)}{2(V_{bi} - V_a)}} = \sqrt{\frac{q\varepsilon A(N_D^+ - n_T(t))}{2(V_{bi} - V_a)}} \tag{3.6}$$

where A is the device area, U is the applied voltage, V_{bi} is the built-in potential, V_a represents the applied bias and $\rho(t)$ is the total charge density inside the

depletion region. Relating the capacitance $C(t)$ to the reverse-bias capacitance (at $-V_R$) of the device without deep-levels C_0 we have:

$$C(t) = C_0\sqrt{1-\frac{n_T(t)}{N_D^+}} \approx C_0\left(1-\frac{n_T(t)}{2N_D^+}\right) \tag{3.7}$$

For majority carrier emission from traps the capacitance transient becomes:

$$C(t) = C_0\left(1-\frac{n_T(0)}{2N_D^+}e^{-e_n t}\right) \tag{3.8}$$

Therefore, the capacitance follows an exponential decay with the same time constant $\tau_e = 1/e_n$ as the trap occupancy does.

The standard DLTS (also called boxcar DLTS) uses a rate window in which the transient is measured. Following a bias pulse, the transient is measured at times t_1 and t_2. Since the transient is temperature dependent, both the sample temperature and the rate window are varied during the experiment. The variation of $C(t_1)$-$C(t_2)$ with temperature is sampled as shown in Fig. 3.4.

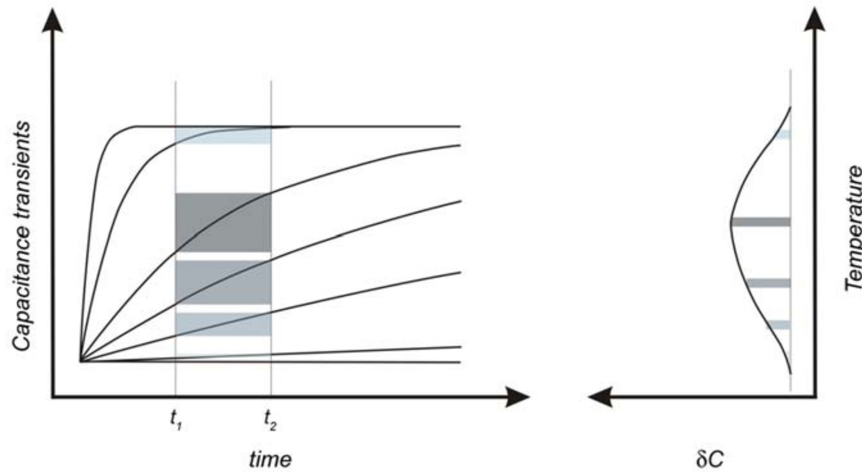

Figure 3.4: Capacitance transients and the corresponding DLTS spectrum.

There is no difference between the capacitance at the two sampling times for very slow or very fast transients, corresponding to low and high temperatures. A difference signal is generated when the time constant τ_e is on the order of (t_2-t_1), and the capacitance difference passes through a maximum giving the DLTS peak. The capacitance difference is expressed as:

$$\delta C = C(t_1) - C(t_2) = \frac{C_0 n_T(0)}{2N_D^+}\left(e^{-\frac{t_2}{\tau_e}} - e^{-\frac{t_1}{\tau_e}}\right) \tag{3.9}$$

In order to determine the value of τ_e for which δC attains a maximum, one has to differentiate δC with respect to τ_e and set the results equal to zero which gives:

$$\tau_{e,\max} = \frac{t_2 - t_1}{\ln\left(\frac{t_2}{t_1}\right)} \tag{3.10}$$

By measuring a series of capacitance transients at different temperatures for a given t_1, t_2 pair, one value of τ_e corresponding to a particular temperature is generated, giving one point on a $ln(\tau_e T^2)$ vs. $1/T$ plot. Repeating the measurement sequence for different t_1 and t_2 a series of points are obtained to generate an Arrhenius plot, which leads to the determination of E_T.

The total trap concentration can be determined from δC setting $t_1=0$ and $t_2=\infty$ in (3.9):

$$N_T = 2N_D^+ \frac{\delta C}{C_0} \tag{3.11}$$

In this work, conventional DLTS measurements were carried out by scanning the temperature between 77 K and 300 K and recording both the capacitance transients and DLTS spectra. The sample preparation and mounting was similar to the procedure described in Section 3.6.1.

The DLTS apparatus at MPI Halle was developed by Dr. O. Breitenstein. The samples were connected to a preamplifier which fed the signal to a C-meter that allows the compensation of the basic capacitance C as well as the conductance G, provided that the capacitance doesn't exceed 500 pF and the resistance is greater than 500 Ω. A sensitivity of 0.5 pF/V was used for all measurements. In the standard operating mode an rf signal (1 MHz) of 100 mV pk-pk (30 mV rms) was applied for the rf capacitance measurement giving a sensitivity of 10^{-4} pF. An additional setting of 1 V pk-pk allowed sensitivities as high as 10^{-5} pF to be attained. The reverse bias and pulse bias could be set between 0 and 15 V.

The capacitance transients were recorded and later processed to calculate the DLTS signal $\delta C=C(t_1)-C(t_2)$ corresponding to eight different rate windows between 1 s^{-1} and 10^4 s^{-1}. Each capacitance transient corresponding to eight values of the filling pulse between 10 μs and 100 ms was recorded, generating an 8x8 matrix of DLTS spectra per measured temperature.

3.7. TEM investigations

The bonded interfaces were examined with the help of transmission electron microscopy (TEM). At MPI Halle two transmission electron microscopes were used: a Philips CM 20 Twin having an accelerating voltage of 200 kV and a high resolution Jeol 4010 with an accelerating voltage of 400 kV. The bonded interfaces were examined in cross-section and in the 25° cut plan-view [105].

For the preparation of the latter, the wafer is sawed in such a way that the bonded interface and the cut form an angle of 25° as depicted in Fig. 3.5. This mode is called plan-view because during the investigation the sample is tilted with 25°, a normal projection of the interface being imaged.

The cross-section samples were prepared by cutting small pieces from the wafer pairs (5x5 mm^2 large) and stabilizing them on 1.5 mm thick silicon pieces. A diamond wire saw was used in order to cut 500 µm thick slices perpendicularly to the interface.

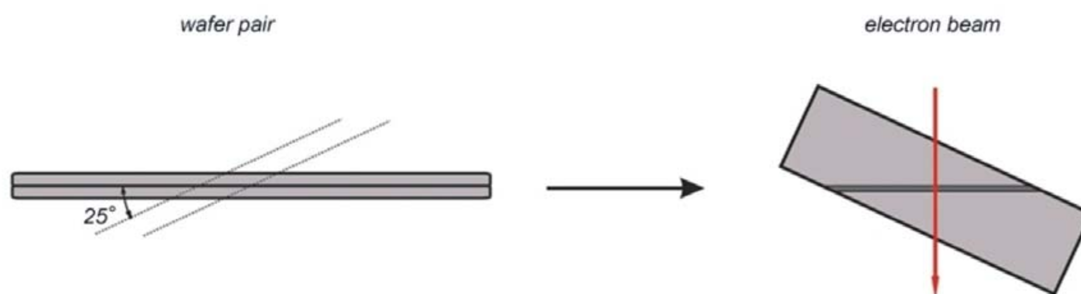

Figure 3.5: Cutting and TEM investigation of a 25° sample.

After gluing with two component epoxy, the slices were bored using a 3 mm ultrasonic drill and underwent polishing/grinding until the thickness reached ca. 10 µm. In the last step, the central part of the sample was further thinned down using a 4 kV PIPS (Precision Ion Polishing System), until a small hole appeared. According to [8], only samples having bonding energies higher than 800 mJ/m^2 can withstand the preparation.

3.8. LEED investigations

In order to study the structure of wafer surfaces at different processing stages, a low-energy electron diffraction (LEED) technique was used [106], [107]. The LEED system consists of three main components: an electron gun, a sample holder and a detector. The electrons were thermally emitted from a LaB_6 cathode (which has a low work function) and were accelerated by a variable voltage to energies between 10 and 200 eV. A system of electrostatic lenses within the gun formed an almost parallel beam which was directed onto the wafer under normal incidence.

The low-energy electrons provided by the electron gun have wavelengths comparable to the atomic spacing on the crystal surface (ca. one Angstrom). Therefore, they may diffract from the surface atoms, i. e. they are elastically back-scattered. Since the cross section for scattering of low-energy electrons is very large, an incident electron beam attenuates within the top few surface layers. These elastically and inelastically scattered electrons propagate in a field-free region between the sample and a transparent metallic grid. Before entering a detector the elastically scattered (i.e. diffracted) electrons have to be separated from the ones that have been inelastically scattered. This is done by a retarding field analyzer which consists of several hemispherical grids. The last

grid is followed by a fluorescent screen onto which the diffracted electrons are once again accelerated by a voltage of 5 kV. Beams appear on the screen as fluorescing spots, and the arrangement of beam spots forms the LEED pattern. This pattern caused by diffraction is an image of the surface reciprocal-lattice.