Silicon Nanowires: Synthesis, Fundamental Issues, and a First Device

Dissertation

t zur Erlangung des akademischen Grades

doctor rerum naturalium (Dr. rer. nat.)

vorgelegt der

Mathematisch-Naturwissenschaftlich-Technischen Fakultät
(matematisch-naturwissenschaftlicher Bereich)
der Martin-Luther-Universität Halle-Wittenberg

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geboren am 28. Juni 1977 in Braunschweig

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Halle (Saale), den 28.5.2006
verteidigt am 13.12.2006

urn:nbn:de:gbv:3-000011060
[http://nbn-resolving.de/urn/resolver.pl?urn=nbn%3Ade%3Agbv%3A3-000011060]
Preface

The purpose of this thesis is to illuminate several aspects regarding the synthesis of silicon nanowires, their electrical properties, and the fabrication of a first device made thereof. Following an introductory survey of important results in silicon nanowire research, Chapter 1 deals with silicon nanowire growth from an experimental point of view. After a detailed description of the experimental setup, the wafer preparation, and the growth procedure, experimental results concerning the epitaxial growth of silicon nanowires with gold are presented. Gold is presently the standard catalyst material for silicon nanowire growth. Yet, serious concerns exist, whether silicon nanowires grown with gold as catalyst can ever become compatible with existing electronics fabrication technology. Therefore, replacing gold by an alternative catalyst material is of great importance. In the second half of Chapter 1 we present silicon nanowire growth results using different catalyst materials: palladium, iron, dysprosium, bismuth, indium, and aluminum.

The three chapters following thereupon each addresses a fundamental silicon nanowire growth issue. Chapter 2 is devoted to the diameter dependence of the silicon nanowire growth velocity. Since the silicon nanowire length is usually controlled by adjusting the growth time, a knowledge of the factors that determine the growth velocity is crucial. Concerning the diameter dependence of the growth velocity, seemingly contradictory observations were made by different groups. Considering the steady state supersaturation of the catalyst droplet we will derive a model that conclusively explains the differences in the observed behavior. Furthermore, our model links the pressure dependence of the growth velocity to the diameter dependence of the growth velocity; an insight that might be useful for an optimization of the growth conditions. Focus of Chapter 3 is on the diameter increase at the nanowire base that can be observed for nanowires grown via the vapor-liquid-solid mechanism on a solid substrate. An explanation for this phenomenon is given in terms of a model that takes the shape of the catalyst droplet into account. In addition, the influence of the line tension on the nanowire morphology is discussed. Chapter 4 deals with the crystallographic growth direction of silicon nanowires, a parameter that is of great importance especially in view of the technical applicability of epitaxially grown silicon nanowires. Experimental results presented in this chapter indicate a diameter-dependent change of the growth direction. We will propose a possible explanation for this growth direction change by taking the interplay of the surface and interface tensions of silicon nanowires into account.

After these partially theoretical considerations with regard to the nanowire morphol-
ogy, the electrical properties of silicon nanowires will be subject of Chapter 5. In the beginning of this chapter we will derive a model for the dependence of the charge carrier density of a silicon nanowire on the density of interface traps and interface charges located at the Si/SiO$_2$ interface. Subsequently, temperature-dependent electrical measurements of both p-doped and n-doped silicon nanowires are presented and discussed in detail. It will be seen that indeed the influence of interface traps and interface charges on the electrical properties can not be neglected. To some degree, the electrical characterization described in Chapter 5 may be seen as a preparatory work for Chapter 6. Having electronic applications of silicon nanowires in mind, the fabrication of a silicon nanowire field-effect transistor is naturally the first step. In this context, epitaxially grown silicon nanowires offer the decisive advantage that, owing to the vertical arrangement of the nanowires, a transistor gate can be wrapped around the silicon nanowire. In Chapter 6 we will present a process flow for the fabrication of an array of vertical surround-gate field-effect transistors out of epitaxially grown silicon nanowires. The feasibility of the fabrication process and the basic functionality of the devices is at last demonstrated by an electrical characterization of such an array of silicon nanowire surround-gate field-effect transistors.

For the convenience of the reader, magnified versions of all graphs are reproduced in the appendix.
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